C2 cont.

28. (New) A semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2, and formed in the substrate, underneath a gate oxide and between a source region and a drain region.

29. (New) The transistor of claim 28, wherein the silicon/germanium (Si-Ge) semiconductor transistor is a p-channel metal-oxide-semiconductor transistor.

Sub. C3

30. (New) A transistor on a silicon substrate, wherein the transistor includes a channel comprising a silicon-germanium (Si-Ge) alloy.

B1 cont.

31. (New) The transistor of claim 30, wherein the channel region has a thickness of approximately 100 to 1000 angstroms.

Sub. C4

32. (New) The transistor of claim 30, wherein, the Si-Ge alloy was formed by a process comprising:

ion implanting Ge ions through a gate oxide on the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge was implanted at an energy of approximately 20 to 100 keV; and

annealing the substrate in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

33. (New) A p-channel metal-oxide semiconductor (PMOS) field effect transistor formed on a substrate, comprising:

a silicon-germanium to silicon ($Si_{1-x}Ge_x$/Si) heterojunction, wherein the germanium (Ge) in the heterojunction has a molar fraction of x.

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34. (New) The PMOS transistor of claim 33, wherein the Ge has a molar fraction of 0.2.

35. (New) The PMOS transistor of claim 33, wherein the silicon-germanium to silicon ($Si_{1-x}Ge_x$/Si) heterojunction includes a $Si_{1-x}Ge_x$ channel region formed on an n- doped silicon substrate.

B1 cont.

36. (New) The PMOS transistor of claim 33, wherein the silicon-germanium to silicon ($Si_{1-x}Ge_x$/Si) heterojunction includes a $Si_{1-x}Ge_x$ channel region formed on an n- doped silicon well formed in a p- doped silicon substrate.

37. (New) A transistor on a silicon substrate, wherein the transistor includes a channel comprising a silicon-germanium (Si-Ge) alloy, and wherein the Si-Ge alloy was formed by a process comprising:

ion implanting germanium (Ge) ions through a gate oxide layer on the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge was implanted at an energy of approximately 20 to 100 keV; and

annealing the substrate in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **September 29 1998**.

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